REMARKS

The Examiner rejected claims 9, 11, 13, 21, 23, 25-26, 28 and 31-32 under 35 U.S.C. §103(a) as allegedly being unpatentable over Fillion et al. (U.S. Pat. 5353498) in view of Nagarajan et al. (U.S. Pat. 6639321).

In response to the Interview Summary dated April 14, 2004 for the interview conducted on March 30, 2004 with the Examiner, Applicants acknowledge that the Interview Summary is accurate.

Applicants respectfully traverse the §103 rejections with the following arguments.

35 U.S.C. §103

The Examiner rejected claims 9, 11, 13, 21, 23, 25-26, 28 and 31-32 under 35 U.S.C. §103(a) as allegedly being unpatentable over Fillion et al. (U.S. Pat. 5353498) in view of Nagarajan et al. (U.S. Pat. 6639321).

The Examiner alleges that "Regarding claims 9 and 25, Fillion et al. disclose a semiconductor device comprising:

a substrate 10, wherein the substrate is selected from the group consisting of a ceramic chip carrier, an organic chip carrier (fig. 1a, column 5, lines 16-18);

a semiconductor device 14 electrically coupled to the substrate, wherein the semiconductor device is divided into a plurality of segments, wherein at least one segment of the plurality of segments is not congruent with respect to a remaining segment of the plurality of segments.

Fillion et al. fail to disclose the substrate comprises a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of the semiconductor device. Nagarajan et al. disclose a semiconductor device (cover fig.) comprising: a substrate 108 comprises a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of the semiconductor device 202 (column 5, lines 1923). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Fillion et al. to reduce mismatch of a coefficient of thermal expansion of the die with the substrate, as shown by Nagarajan et al".

As to claim 9, Applicants contend that the rejection of claim 9 under 35 U.S.C. §103(a) as allegedly being unpatentable over Fillion et al. in view of Nagarajan et al. is improper because

Applicants respectfully contend that the Examiner has not provided a persuasive reason for modifying Fillion by the alleged teaching of Nagarajan for rejecting claim 9. The only basis that the Examiner provides for modifying Fillion with Nagarajan is that Nagarajan teaches a substrate 108 comprising a coefficient of thermal expansion greater that a coefficient of thermal expansion of a semiconductor device 202. The Examiner alleges that " it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Fillion et al. to reduce mismatch of a coefficient of thermal expansion of the die with the substrate, as shown by Nagarajan et al ". In response, Applicants contend that Nagarajan does not teach an advantage to having a coefficient of thermal expansion (CTE) of a substrate that is greater than a CTE of a semiconductor device (i.e., a CTE mismatch) as taught by Applicant's claim 9. In fact, Nagarajan actually teaches away from having a CTE of a substrate that is greater than a CTE of a semiconductor device. For example in col. 1, lines 24-26, Nagarajan teaches that there are stresses on a semiconductor device (die 106) due to a CTE mismatch (e.g.,CTE of a substrate greater than a CTE of a semiconductor device) between a semiconductor device (die 106) and a substrate (substrate 108). Nagarajan continues to teach in col. 1, lines 46-47 that the CTE mismatch causes poor adhesion between an adhesive underfill and a passivation. Thus Nagarajan teaches that having the CTE of the substrate exceed the CTE of the semiconductor device causes problems. Thus, Applicants maintain that the Examiner has not persuasively demonstrated that it is obvious to modify Fillion with Nagarajan. Accordingly, Applicants contend that the Examiner has not disclosed a teaching or suggestion in the prior art that supports the modification. Therefore, Applicants contend that Fillion and Nagarajan may not be combined for the purpose of rejecting claim 9. Based on the preceding arguments,

Applicants respectfully maintain that claim 9 is not unpatentable over Fillion in view of Nagarajan, and that claim 9 is in condition for allowance. Since claims 10, 11, 13, 21, and 23 depend from claim 9, Applicants contend that claims 10, 11, 13, 21, and 23 are likewise in condition for allowance.

As to claim 25, Applicants respectfully contend that claim 25 is not unpatentable over Fillion in view of Nagarajan, because Fillion and Nagarajan do not individually or collectively teach or suggest each and every feature of claim 25. For example, Fillion and Nagarajan do not teach or suggest the feature of "**dividing** a semiconductor device into a plurality of segments" (emphasis added). Fillion and Nagarajan do not teach or suggest that a semiconductor device is **divided** into a plurality of segments as taught by Applicant's claim 25. In contrast, Fillian teaches a plurality of chips14 **placed** on a surface (e.g., base sheet 12, see Nagarajan, col. 5, lines 22-35, FIG. 1a, and claim 1). Nagarajan do not disclose any method of fabricating the plurality of chips 14 for placement on a surface as taught by Applicant's claim 25 and most certainly does not teach the "dividing" step of claim 25. Therefore Applicant's contend that Fillion and Nagarajan do not teach or suggest the preceding features of claim 25. Based on the preceding arguments, Applicants respectfully maintain that claim 25 is not unpatentable over Fillion in view of Nagarajan, and that claim 25 is in condition for allowance. Based on the preceding arguments, Applicants respectfully maintain that claim 25 is not unpatentable over Fillion in view of Nagarajan, and that claim 25 is in condition for allowance. Since claims 26, 28, and 31-32 depend from claim 25, Applicants contend that claims 26, 28, and 31-32 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below.

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Jack P. Friedman
Registration No. 44,688

Schmeiser, Olsen & Watts
3 Lear Jet Lane, Suite 201
Latham, New York 12110
(518) 220-1850